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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)				ATTY. DOCKET NO. 50099-180	SERIAL NO. 09/988,593		
				APPLICANT Shigenobu MAEDA, et al.			
				FILING DATE November 20, 2001	GROUP 2823		
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code: (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear		
WP		US	5,767,549	08/16/1998	Chen et al.		
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
WP		FR 2 788 883 A1	07/28/2000	MITSUBISHI ELECTRIC CORP		Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
WP		Y. HIRANO, et al. "Bulk Layout Compatible 0.18 μ m SOI CMOS Technology Using Body-Fixed Partial Trench Isolation (PTI)", IEEE International SOI Conference, Oct. 1999.					
EXAMINER <i>Shamir</i>				DATE CONSIDERED 4/2/04			

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